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NASA TECH BRIEF

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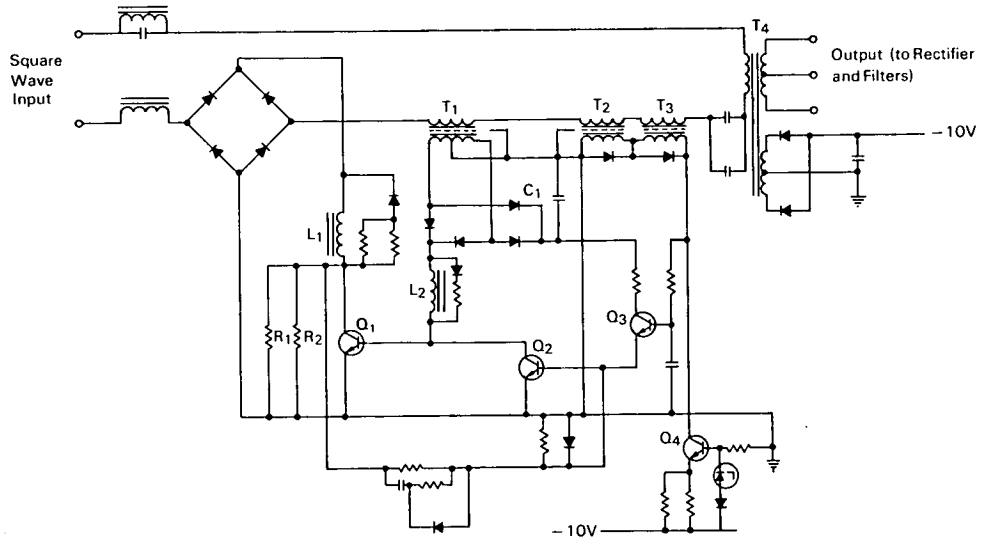
High-Speed Square-Wave Current Limiter Operates Efficiently



The problem: To design a circuit that will operate efficiently at high speed to limit the current from a square-wave ac power supply to a predetermined value.

The solution: A transistorized current limiter in which the transistors operate as switches, resetting after each half cycle of the square wave and thus minimizing power losses.

How it's done: During normal operation when limiting is necessary only for momentary loads, such as square-wave switching transients, the diode bridge directs the input through filter L_1 and transistor Q_1. Filter L_1 acts to limit current transients in the square-wave input much as a series inductor does in a dc line. Transistor Q_1 operates as a switch, and is normally saturated by current transformer T_1 through filter L_2. Current transformer T_1 also provides collector voltage for transistor Q_3 by charging capacitor C_1 with transient voltage spikes.

Transformers T_2 and T_3 are square-loop current transformers which are normally saturated in opposite directions by bias current from transistor Q_4. During a particular half cycle, one of the transformers will be driven out of saturation. If the current is sufficiently high, it will overcome transistor Q_4 bias current and saturate transistor Q_3. Transistor Q_3 drives transistor Q_2 into saturation which, in turn, cuts off transistor Q_1 and directs the square-wave input through current-limiting resistors R_1 and R_2. At the end of the half cycle, the reversal of the square-wave input causes transistor Q_2 to turn off, allowing transistor Q_1 to saturate again. The high impedance of resistors R_1 and R_2 is shunted out and line current is allowed to

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increase until it reaches the predetermined peak whereupon the limiting process repeats. In this way, the current is limited on an instantaneous basis to a predetermined value without producing high losses when the load is normal.

The −10 volt reference to transistor Q_4 is obtained from a winding on output transformer T_4 so that the bias current applied to transformers T_2 and T_3, which determines the limiting current, is a function of the output transformer voltage. An extremely heavy load on the power transformer will cause current limitation even if the instantaneous current is below the normal limiting value.

Notes:

1. An important feature of this invention is that no high power dissipation transistors are required, the operation being such that overheating and possible damage of transistors handling the main line current are avoided.
2. Inquiries concerning this invention may be directed to

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   Reference: B65-10233

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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